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POINTS TO REMEMBER

1. Electronics

A device whose functioning is based on controlled movement of electrons through it is called an electronic device. Some of the present-day most common such devices include a semiconductor junction diode, a transistor and integrated circuits. The related branch in which we study the functioning and use of such devices is called Electronics.

2. Energy Bands in Solids

An isolated atom has well defined energy levels. However, when large number of such atoms get together to form a real solid, these individual energy levels overlap and get completely modified. Instead of discrete value of energy of electrons, the energy values lie in a certain range. The collection of these closely packed energy levels are said to form an energy band. Two types of such bands formed in solids are called Valence Band and Conduction Band. The band formed by filled energy levels is known as Valence Band whereas partially filled or unfilled band is known as Conduction Band. The two bands are generally separated by a gap called energy gap or forbidden gap. Depending upon the size of this energy gap, different materials behave as conductors, semi-conductors or insulators. The insulators have generally large energy gap whereas the conductors do not have any such gap. Semi-conductors have small energy gap.

3. Types of Semi-conductors—Intrinsic and Extrinsic

Common Semiconductors are of two types—intrinsic and extrinsic. Germanium and silicon are two most commonly used semiconductor material.

Intrinsic Semiconductor: Pure semiconductors is in which the conductivity is caused due to charge carriers made available from within the material are called *intrinsic semiconductors*. There are no free charge carriers available under normal conditions. However, when the temperature is raised slightly, some of the covalent bonds in the material get broken due to thermal agitation and few electrons become free. In order to fill the vacancy created by absence of electron at a particular location, electron from other position move to this location and create a vacancy (absence of electron) at another place called *hole*. The movement/shifting of electrons and holes within the material results in conduction.

An intrinsic semiconductors behaves as a perfect insulator at temperature 0 K.

Extrinsic semiconductors: The semiconductors in which the conductivity is caused due to charge carriers made available from external source by adding impurity from outside are called *extrinsic semiconductor*. The process of adding impurity is called *doping*. The impurity added is generally from third group or fifth group. There are two types of extrinsic semiconductors:

(*a*) *n*–Type or (*b*) *p*–Type.

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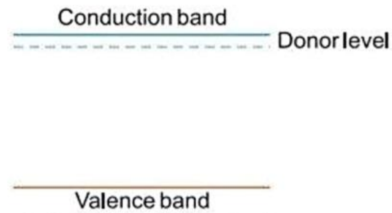
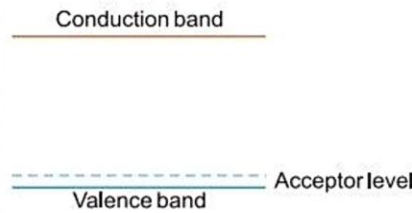
If n_i is the density of intrinsic charge carriers, n_e and n_h are densities of electrons and hole in extrinsic semiconductors, then the selection among them is $n_e n_h = n_i^2$

(*a*) **n-type semiconductors:** When a pentavalent impurity like Phosphorus, Antimony, Arsenic is doped in pure-Germanium (or Silicon), then the conductivity of crystal increases due to surplus electrons and such a crystal is said to be *n*-type semiconductor, while the impurity atoms are called **donors atoms**. Thus, in *n*-type semiconductors the charge carriers are negatively charged electrons and the donor level lies near the bottom of the conduction band.



(*a*) ***n*-type semiconductor**

(*b*) **p-type semiconductors:** When a trivalent impurity like Aluminium, Indium, Boron, Gallium, etc., is doped in pure Germanium (or silicon), then the conductivity of the crystal increases due to deficiency of electrons *i.e.*, holes and such a crystal is said to be *p*–type semiconductor while the impurity atoms are called **acceptors**. Thus in *p*–type semiconductors the charge carriers are holes. Acceptor level lies near the top of the valence band.



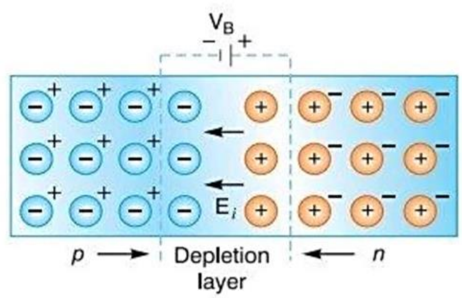
(*b*) ***p*-type semiconductor**

4. Semiconductor Diode: *p-n* Junction Diode

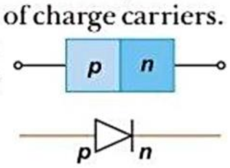
A semiconductor having *p*-type impurity at one end and *n*-type impurity at the other end is known as *p* – *n* junction diode. The junction at which *p*-type and *n*-type semiconductors combine is called *p-n* junction.

In *p*-type region there is majority of holes and in *n*-type region there is majority of electrons.

Formation of Depletion Layer and Potential Barrier



At the junction, there is diffusion of charge carriers due to thermal agitation; therefore some of electrons of *n*-region diffuse to *p*-region while some of holes of *p*-region diffuse into *n*-region. Some charge carriers combine with opposite charges to neutralise each other. Thus, near the junction there is an excess of positively charged ions in *n*-region and an excess of negatively charged ions in *p*-region. This sets up a potential difference called **potential barrier** and hence an internal electric field E_i across the junction. The potential barrier is usually of the order of μV. The field E_i is directed from *n*-region to *p*-region. This field stops the further diffusion of charge carriers. Thus the layers (≈10^{-4} cm to 10^{-6} cm) on either side of the junction becomes free from mobile charge carriers and hence is called the *depletion layer.* The symbol of *p-n* junction diode is shown in figure.



Forward and Reverse Bias

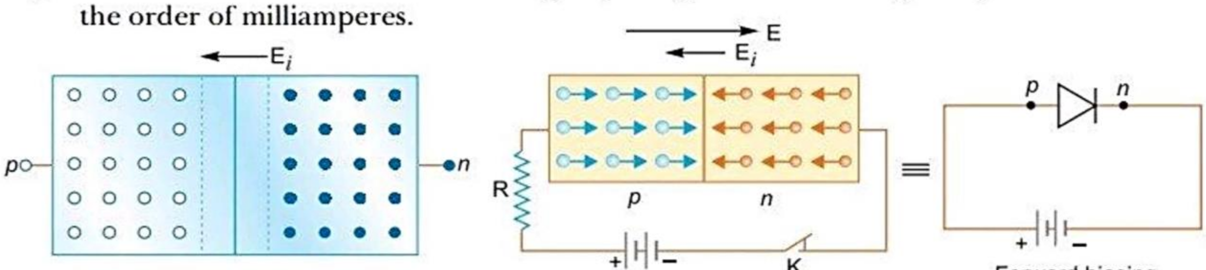
The external battery is connected across the junction in the following two ways:

(*i*) **Forward Bias:** In this arrangement the positive terminal of battery is connected to *p*-end and negative terminal to *n*-end of the crystal, so that an external electric field *E* is established directed from *p* to *n*-end to oppose the internal field E_i. Thus, the junction is said to conduct.

Under this arrangement the holes move along the field *E* from *p*-region to *n*-region and electrons move opposite to field *E* from *n*-region to *p*-region; eliminating the depletion layer. A current is thus set up in the junction diode. The following are the basic features of forward biasing:

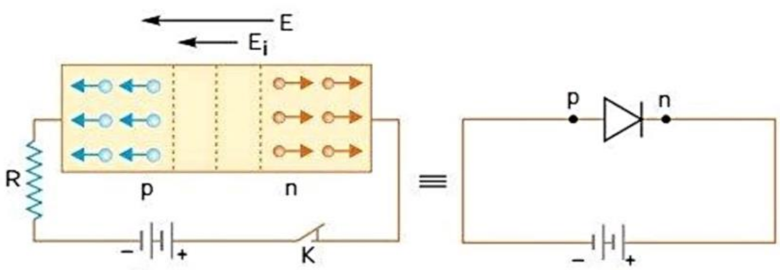
(*a*) Within the junction diode the current is due to both types of majority charge carriers but in external circuit it is due to electrons only.

(b) The current is due to diffusion of majority charge carriers through the junction and is of the order of milliamperes.



(a) No current (b) Forward current Forward biasing

(ii) Reverse Bias: In this arrangement the positive terminal of battery is connected to *n*-end and negative terminal to *p*-end of the crystal, so that the external field is established to support the internal field E_i as shown in fig. Under the biasing the holes in *p*-region and the electrons in *n*-region are pushed away from the junction to widen the depletion layer and hence increases the size of the potential barrier, therefore, the junction does not conduct.



(c) Reverse current Reverse biasing

When the potential difference across the junction is increased in steps, a very small reverse current of the order to micro-amperes flows. The reason is that due to thermal agitation some covalent bonds of pure semi-conductor break releasing a few holes in *n*-region and a few electrons in *p*-region called the *minority charge carriers*. The reverse bias opposes the majority charge carriers but aids the minority charge carriers to move across the junction. Hence a very small current flows.

The basic features of reverse bias are:

(a) Within the junction diode the current is due to both types of minority charge carriers but in external circuit it is due to electrons only.

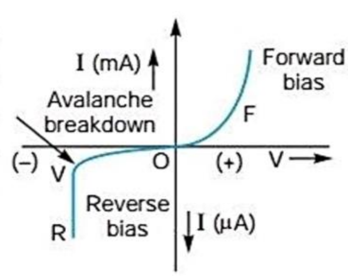
(b) The current is due to leakage of minority charge carriers through the junction and is very small of the order of μA.

Characteristics of a *p–n* junction diode:

The graph of voltage *V* versus current *I* in forward bias and reverse bias of a *p–n* junction is shown in the figure.

Avalanche Break Down:

If the reverse bias is made sufficiently high, the covalent bonds near the junction break down releasing free electrons and holes. These electrons and holes gain sufficient energy to break other covalent bonds. Thus a large number of electrons and holes get free. The reverse current increases abruptly to high value. This is called avalanche break down and may damage the junction.

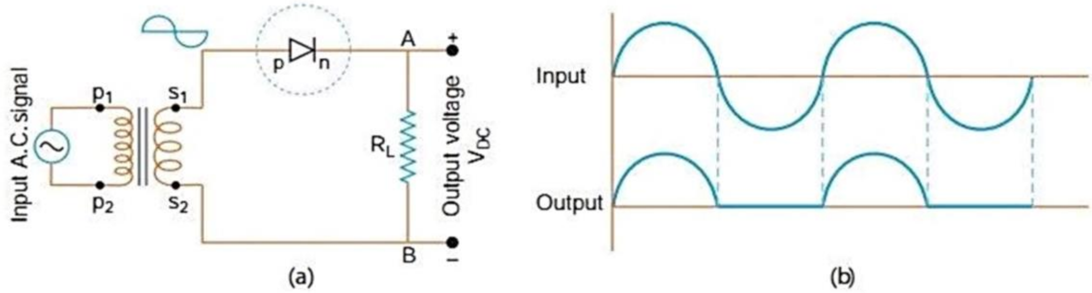


5. *p-n* Junction Diode as a Half-wave Rectifier

The conversion of ac into dc is called the rectification.

POINTS TO REMEMBER

Half Wave Rectifier: The circuit diagram for junction diode as half wave rectifier is shown in fig. (*a*)

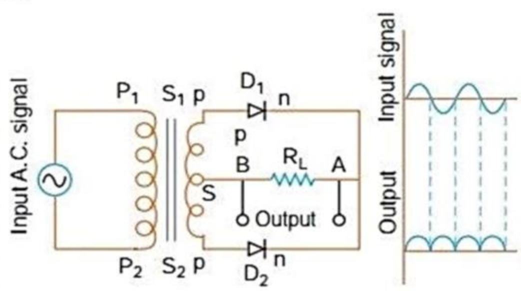


During first half of the input cycle, the secondary terminal S_1 of transformer be positive relative to S_2 then the junction diode is forward biased. Therefore, the current flows and its direction of current in load resistance R_L is from A to B. In next half cycle, the terminal S_1 becomes negative relative to S_2, then the diode is in reverse bias, therefore no current flows in diode and hence there is no potential difference across load R_L. The cycle repeats. The output current in load flows only when S_1 is positive relative to S_2 That is during first half cycles of input ac signal there is a current in circuit and hence a potential difference across load resistance R_L while no current flows, for next half cycle. The direction of current in load is always from A to B which is direct current. Thus, a *single p-n junction diode acts as a half wave rectifier*.

The input and output waveforms of half wave rectifier are shown in fig. (*b*).

Full Wave Rectifier: For full wave rectifier, we use two junction diodes. The circuit diagram for full wave rectifier using two junction diodes is shown in figure.

During first half cycle of input ac signal the terminal S_1 is positive relative to S and S_2 is negative relative to S, then diode D_1 is forward biased and diode D_2 is reverse biased. Therefore current flows in diode D_1 and not in diode D_2. The direction of current i_1 due to diode D_1 in load resistance R_L is directed from A to B. In next half cycle, the terminal S_1 is negative relative to S and S_2 is positive relative to S. Then diode D_1 is reverse biased and diode D_2 is forward biased. Therefore, current flows in diode D_2 and there is no current in diode D_1. The direction of current i_2 due to diode D_2 in load resistance is again from A to B Thus, for input ac signal the output current is a continuous series of unidirectional pulses. The input and output sequels are shown in the figure. This output current can be converted into steady current by the use of suitable filters.



Remark: In full wave rectifier if the fundamental frequency of input ac signal is 50 Hz, then the fundamental frequency of output is 100 Hz.

COMPETENCY-FOCUSED QUESTIONS AS PER NEP

Multiple Choice Questions

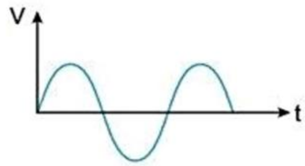
Choose and write the correct option(s) in the following questions.

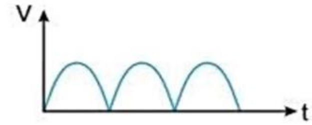
1. **When an intrinsic semiconductor is doped with a small amount of trivalent impurity, then** [*CBSE 2023 (55/1/1)*]
   (*a*) its resistance increases
   (*b*) it becomes a *p*-type semiconductor
   (*c*) there will be more free electrons than holes in the semiconductor
   (*d*) dopant atoms become donor atoms.

2. In the energy-band diagram of *n*-type Si, the gap between the bottom of the conduction band E_C and the donor energy level E_D is of the order of *[CBSE 2023 (55/1/1)]*

(*a*) 10 eV (*b*) 1eV (*c*) 0.1 eV (*d*) 0.01 eV

3. An *ac* source of voltage is connected in series with a *p-n* junction diode and a load resistor. The correct option for output voltage across load resistance will be *[CBSE 2023 (55/1/1)]*

(*a*)


(*b*)


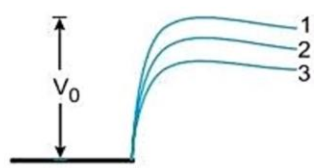
(*c*)


(*d*)


4. The conductivity of a semiconductor increases with increase in temperature because *[NCERT Exemplar]*

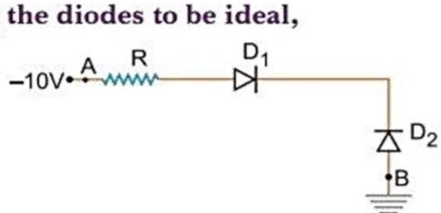
(*a*) number density of free current carriers increases.
(*b*) relaxation time increases.
(*c*) both number density of carriers and relaxation time increase.
(*d*) number density of current carriers increases, relaxation time decreases but effect of decrease in relaxation time is much less than increase in number density.

5. In given figure, V_0 is the potential barrier across a *p-n* junction, when no battery is connected across the junction *[NCERT Exemplar]*



(*a*) 1 and 3 both correspond to forward bias of junction
(*b*) 3 corresponds to forward bias of junction and 1 corresponds to reverse bias of junction
(*c*) 1 corresponds to forward bias and 3 corresponds to reverse bias of junction.
(*d*) 3 and 1 both correspond to reverse bias of junction.

6. In given figure, assuming the diodes to be ideal, *[NCERT Exemplar]*



(*a*) D_1 is forward biased and D_2 is reverse biased and hence currentflows from *A* to *B*.
(*b*) D_2 is forward biased and D_1 is reverse biased and hence no current flows from *B* to *A* and vice versa.
(*c*) D_1 and D_2 are both forward biased and hence current flows from *A* to *B*.
(*d*) D_1 and D_2 are both reverse biased and hence no current flows from *A* to *B* and vice versa.

7. In an extrinsic semiconductor, the number density of holes is 4×10^{20} m^{-3}. If the number density of intrinsic carriers is 1.2×10^{15} m^{-3} the number density of electrons in it is *[CBSE 2023 (55/2/1)]*

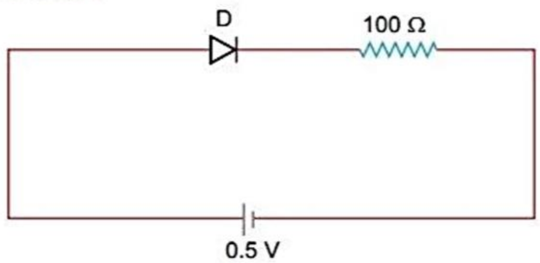
(*a*) 1.8×10^9 m^{-3} (*b*) 2.4×10^{10} m^{-3}
(*c*) 3.6×10^9 m^{-3} (*d*) 3.2×10^{10} m^{-3}

8. **At a certain temperature in an intrinsic semiconductor the electrons and holes concentration is 1.5×10^{-16} m^{-3}. When it is doped with a trivalent dopant, hole concentration increases to 4.5×10^{-22} m^{-3}. In the doped semiconductor, the concentration of electrons (*ne*) will be** **[*CBSE 2023 (55/3/1)*]**
   (*a*) 3×10^{6} m^{-3} (*b*) 5×10^{7} m^{-3}
   (*c*) 5×10^{9} m^{-3} (*d*) 6.75×10^{38} m^{-3}

9. **When an electric field is applied across a semiconductor** **[*NCERT Exemplar*]**
   (*a*) electrons move from lower energy level to higher energy level in the conduction band.
   (*b*) electrons move from higher energy level to lower energy level in the conduction band.
   (*c*) holes in the valence band move from higher energy level to lower energy level.
   (*d*) holes in the valence band move from lower energy level to higher energy level.

10. **When trivalent impurity is mixed in a pure semiconductor, the conduction is mainly due to**
   (*a*) electrons (*b*) holes
   (*c*) protons (*d*) positive ions

11. **The threshold voltage for a *p-n* junction diode used in the circuit is 0.7 V. The type of biasing and current in the circuit are:** **[*CBSE 2023 (55/4/1)*]**

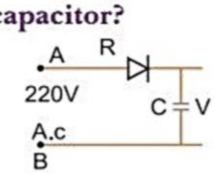


   (*a*) Forward biasing, 0 A (*b*) Reverse biasing, 0 A
   (*c*) Forward biasing, 5 mA (*b*) Reverse biasing, 2 mA

12. **The impurity atoms to be mixed in pure silicon to form *p*-type semiconductor are, of**
   (*a*) phosphorus (*b*) germanium
   (*c*) antimony (*d*) aluminium

13. **Holes are charge carriers in**
   (*a*) intrinsic semiconductor only (*b*) *p*-type semiconductor only
   (*c*) intrinsic and *p*-type semiconductors (*d*) *n*-type semiconductor

14. **A 220 V *ac* supply is connected between points *A* and *B* (shown in figure). What will be the potential difference *V* across the capacitor?** **[*NCERT Exemplar*]**



   (*a*) 220 V (*b*) 110 V (*c*) 0 V (*d*) $220\sqrt{2}$ V

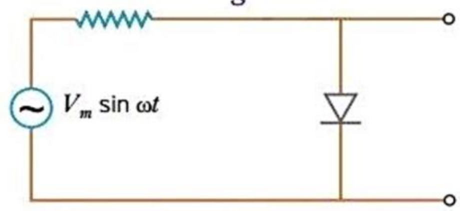
15. **Hole is** **[*NCERT Exemplar*]**
   (*a*) an anti-particle of electron.
   (*b*) a vacancy created when an electron leaves a covalent bond.
   (*c*) absence of free electrons.
   (*d*) an artificially created particle.

16. **In the depletion region of a diode** **[*NCERT Exemplar*]**
   (*a*) there are no mobile charges
   (*b*) equal number of holes and electrons exist, making the region neutral.
   (*c*) recombination of holes and electrons has taken place.
   (*d*) immobile charged ions exist.

17 The breakdown in a reverse biased *p-n* junction diode is more likely to occur due to [*NCERT Exemplar*]

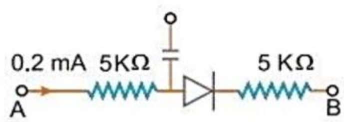
(*a*) large velocity of the minority charge carriers if the doping concentration is small.
(*b*) large velocity of the minority charge carriers if the doping concentration is large.
(*c*) strong electric field in a depletion region if the doping concentration is small.
(*d*) strong electric field in the depletion region if the doping concentration is large.

18. The output of the given circuit shown in figure. [*NCERT Exemplar*]



(*a*) would be zero at all times.
(*b*) would be like a half wave rectifier with positive cycles in output.
(*c*) would be like a half wave rectifier with negative cycles in output.
(*d*) would be like that of a full wave rectifier.

19. In the circuit shown in figure, if the diode forward voltage drop is 0.3 V, the voltage difference between *A* and *B* is [*NCERT Exemplar*]



(*a*) 1.3 V (*b*) 2.3 V (*c*) 0 (*d*) 0.5 V

20. At equilibrium, in a *p-n* junction diode the net current is [*CBSE 2020 (55/2/1)*]

(*a*) due to diffusion of majority charge carriers.
(*b*) due to drift of minority charge carriers.
(*c*) zero as diffusion and drift currents are equal and opposite.
(*d*) zero as no charge carriers cross the junction.

21. In an *n*-type semiconductor, the donor energy level lies [*CBSE 2020 (55/2/1)*]

(*a*) at the centre of the energy gap. (*b*) just below the conduction band.
(*c*) just above the valance band. (*d*) in the conduction band.

22. The manifestation of band structure in solids is due to

(*a*) Heisenberg's uncertainty principle (*b*) Pauli's exclusion principle
(*c*) Bohr's correspondence principle (*d*) Boltzmann's law

23. A piece of copper and another of germanium are cooled from room temperature to 77 K. The resistance of [*HOTS*]

(*a*) each of these decreases
(*b*) copper strip increases and that of germanium decreases
(*c*) copper strip decreases and that of germanium increases
(*d*) each of these increases

Answers

1. (*b*)	**2.** (*d*)	**3.** (*c*)	**4.** (*d*)	**5.** (*b*)	**6.** (*b*)	**7.** (*c*)
8. (*c*)	**9.** (*a*), (*c*)	**10.** (*b*)	**11.** (*a*)	**12.** (*d*)	**13.** (*c*)	**14.** (*d*)
15. (*b*)	**16.** (*a*), (*b*), (*d*)	**17.** (*a*), (*d*)	**18.** (*c*)	**19.** (*b*)	**20.** (*c*)	**21.** (*b*)
22. (*b*)	**23.** (*c*)					

AS PER NEP COMPETENCY-FOCUSED QUESTIONS

Assertion-Reason Questions

In the following questions, a statement of Assertion (A) is followed by a statement of Reason (R). Choose the correct answer out of the following choices.

(a) *Both A and R are true and R is the correct explanation of A.*

(b) *Both A and R are true but R is not the correct explanation of A.*

(c) *A is true but R is false.*

(d) *A is false and R is also false.*

1. **Assertion** (*A*) : A pure semiconductor has negative temperature coefficient of resistance.

   Reason (*R*) : On raising the temperature, more charge carriers are released, conductance increases and resistance decreases. [*AIIMS 2010*]

2. **Assertion** (*A*) : In '*n*' type semiconductor, number density of electrons is greater than the number density of holes but the crystal maintains an overall charge neutrality.

   Reason (*R*) : The charge of electrons donated by donor atoms is just equal and opposite to that of the ionised donor. [*CBSE 2023 (55/4/1)*]

3. **Assertion** (*A*) : The forbidden energy gap between the valence and conduction bands is greater in silicon than in germanium.

   Reason (*R*) : Thermal energy produces fewer minority carriers in silicon than in germanium.

4. **Assertion** (*A*) : When the temperature of a semiconductor is increased, then its resistance decreases.

   Reason (*R*) : The energy gap between valence and conduction bands is very small for semiconductors.

5. **Assertion** (*A*) : The electrical conductivity of *n*-type semiconductor is higher than that of *p*-type semiconductor at a given temperature and voltage applied.

   Reason (*R*) : The mobility of electron is higher than that of hole.

6. **Assertion** (*A*) : A *p*-type semiconductor has negative charge on it.

   Reason (*R*) : *p*-type impurity atom has positive charge carrier (electrons) in it.

7. **Assertion** (*A*) : The energy gap between the valence band and conduction band is greater in silicon than in germanium.

   Reason (*R*) : Thermal energy produces fewer minority carriers in silicon than in germanium.

8. **Assertion** (*A*) : The temperature coefficient of resistance is positive for metals and negative for *p*-type semiconductors.

   Reason (*R*) : The effective charge carriers in metals are negatively charged electrons, whereas in *p*-type semiconductors, they are positively charged.

9. **Assertion** (*A*) : Diamond behaves such as an insulator.

   Reason (*R*) : There is a large energy gap between valence band and conduction bond of diamond.

10. **Assertion** (*A*) : At a fixed temperature, silicon will have a minimum conductivity when it has a smaller acceptor doping.

    Reason (*R*) : The conductivity of an intrinsic semiconductor is slightly higher than that of a lightly doped *p*-type. [*AIIMS 2010*]

Answers

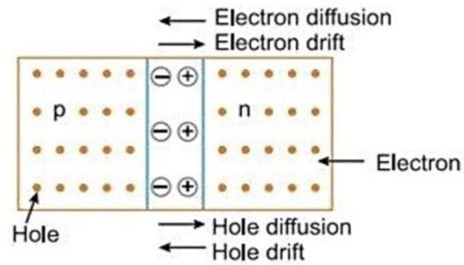
1. (*b*) **2.** (*a*) **3.** (*b*) **4.** (*a*) **5.** (*a*) **6.** (*d*) **7.** (*a*)
8. (*a*) **9.** (*a*) **10.** (*a*)

COMPETENCY-FOCUSED QUESTIONS AS PER NEP

Case-based/Passage-based Questions

Read the paragraph given below and answer the questions that follow:

Motions of the Charge Carriers: If you burst a helium -filled balloon, helium atoms will diffuse (spread) outward into the surrounding air. This happens because these are very few helium atoms in normal air. In more formal language, there is a helium density gradient at the balloon-air interface (the number density of helium atoms varies across the interface), the helium atoms move so as to reduce the gradient.



In same way, electrons on the *n*-side are close to the junction plane tend to diffuse across it and into the *p*-side, where there are very few free electrons. Similarly, holes on the *p*-side are close to the junction plane tend to diffuse across that plane and into the *n*-side, where there are very few holes. The motions of both the electrons and the holes contribute to a diffusion current ($I_{diff.}$).

(*i*) **Silicon is doped with which of the following to obtain *p*-type semiconductor?**

(*a*) Phosphorus (*b*) Gallium
(*d*) Germanium (*a*) Bismuth

(*ii*) **A semiconductor has an electron concentration of 6×10^{22} per m^3 and hole concentration of 8.5×10^9 per m^3. Then it is**

(*a*) *n*-type semiconductor (*b*) *p*-type semi conductor
(*c*) intrinsic semiconductor (*d*) conductor

(*iii*) **In a *p-n*-junction diode**

(*a*) the current in the reverse biased condition is generally very small ~ μA
(*b*) the current in the reverse biased condition is small but the forward biased current is independent of the bias voltage
(*c*) the reverse biased current is strongly dependent on the applied voltage
(*d*) the forward biased current is very small in comparison to reverse biased current

(*iv*) **In the middle of the depletion layer of a reverse biased *p-n* junction, the**

(*a*) electric field is zero (*b*) potential is maximum
(*c*) electric field is maximum (*d*) potential is zero

OR

The dominant mechanism for the motion of charge carriers in forward and reverse biased silicon junctions are

(*a*) drift in forward bias, diffusion in reverse bias
(*b*) diffusion in forward bias, drift in reverse bias
(*c*) diffusion in both forward and reverse bias
(*d*) drift in both forward and reverse bias

Explanations

(i) (b) Gallium being trivalent atom makes *p*-type semiconductor.

(ii) (a) The given semiconductor is *n*-type semiconductor as e^- concentration > hole concentration.

(iii) (a) In forward biased *p-n*-junction, external voltage decreases the potential barrier, so current is maximum. While in reversed biased *p-n*-junction, external voltage increases the potential barrier, so the current is very small of the order μA.

(iv) (a) When *p-n* junction is reversed biased, the width of the depletion layer becomes large and so, the electric field $\left(E = \frac{v}{d}\right)$ becomes very small, nearly zero.

(v) (b) diffusion in forward bias, drift in reverse bias.

CONCEPTUAL QUESTIONS

Q. 1. Name two intrinsic semiconductors.

Ans. Germanium, silicon

Q. 2. Name charge carriers in *p*-type semiconductor.

Ans. Holes.

Q. 3. Name charge carriers in *n*-type semiconductor.

Ans. Free electrons

Q. 4. If n_i is density of intrinsic charge carriers; n_h and n_e are densities of hole and electrons in extrinsic semiconductor, what is the relation among them?

Ans. $n_e n_h = n_i^2$

Q. 5. What is the net charge on (i) *p*-type semiconductor (ii) *n*-type semiconductor?

Ans. (i) Zero (ii) Zero

Q. 6. Why cannot we use Si and Ge in fabrication of visible LEDs? [*CBSE 2020 (55/1/1)*]

Ans. Si & Ge cannot be used for fabrication of visible LED because their energy gap is less 1.8 eV [*CBSE Marking Scheme 2020 (55/1/1)*] 1

Q. 7. How does the width of depletion region of a *p–n* junction vary if doping concentration is increased? [*CBSE Sample Paper 2021*]

Ans. When doping concentration is kept high in *p–n* junction, then there will be less space for electron to travel and equilibrium is achieved by recombination between charge carriers in nearby region. So, depletion width is decreased with doping.

Q. 8. At what temperature would an intrinsic semiconductor behave like a perfect insulator? [*CBSE East 2010*]

Ans. An intrinsic semiconductor behaves as a perfect insulator at temperature 0 K.

Q. 9. Can a slab of *p*-type semi-conductor be physically joined to another *n*-type semiconductor slab to form *p-n* junction? Justify your answer. [*CBSE 2020 (55/4/1)*]

Ans. No, slab will have roughness much larger than the inter atoms crystal spacing and hence continuous contact at the atomic level will not be possible. The junction will behave as a discontinuity for the flowing charge carriers. [*CBSE Marking Scheme 2020 (55/4/1)*] 1

Q. 10. What type of extrinsic semiconductor is formed when
(i) germanium is doped with indium?
(ii) silicon is doped with bismuth?

Ans. (i) Indium is trivalent, so germanium doped indium is a *p*-type semiconductor.
(ii) Bismuth is pentavalent, so silicon doped bismuth is an *n*-type semiconductor.

Q. 11. What happens to the width of depletion layer of a *p-n* junction when it is (*i*) forward biased, (*ii*) reverse biased? [*CBSE Delhi 2011*]

Ans. (*i*) When forward biased, the width of depletion layer decreases.

(*ii*) When reverse biased, the width of depletion layer increases.

Q. 12. In a *p-n* junction diode the forward bias resistance is low as compared to the reverse bias resistance. Give reason. [*CBSE 2020 (55/4/1)*]

Ans. In a *p-n* junction diode the forward bias has a low resistance because the barrier potential decreases and when the diode is reverse biased then the barrier potential increases hence it has a high resistance. [*CBSE Marking Scheme 2020 (55/4/1)*] 1

Q. 13. How are energy bands formed in a crystalline solid?

Ans. Isolated atoms have discrete energy levels. In a crystalline solid, due to the presence of large number of atoms, interatomic interactions take place. Due to this, energy levels get modified to energy bands.

Q. 14. Carbon and silicon have the same lattice structure. Then why is carbon an insulator but silicon a semiconductor? [*CBSE 2023 (55/4/1)*]

Ans. The 4 bonding of electrons of *C* and Si lie respectively, in the second and third orbit. Hence energy required to take out an electron from their atoms will be much less than for *C*. Hence number of free e^- for conduction in Si significant but negligibly small for *C*.

Q. 15. The energy gaps in the energy band diagrams of a conductor, semiconductor and insulator are E_1, E_2 and E_3. Arrange them in increasing order.

Ans. The energy gap in a conductor is zero, in a semiconductor is ≈ 1 eV and in an insulator is ≥ 3 eV.

$\therefore \quad E_1 = 0, E_2 = 1 \text{ eV}, E_3 \geq 3 \text{ eV}$

$\therefore \quad E_1 < E_2 < E_3$

Q. 16. In half wave rectification, what is the output frequency if input frequency is 25 Hz? [*CBSE Sample Paper 2021*]

Ans. For a half wave rectifier, the output frequency is equal to the input frequency. So, the frequency after rectification is 25 Hz.

Q. 17. Can the potential barrier across a *p-n* junction be measured by simply connecting a voltmeter across the junction? [*HOTS*] [*NCERT Exemplar*]

Ans. No, because the voltmeter must have a resistance very high compared to the junction resistance, the latter being nearly infinite.

Q. 18. When a voltage drop across a *p–n* junction diode is increased from 0.70 V to 0.71 V, the change in the diode current is 10 mA .What is the dynamic resistance of diode? [*CBSE Sample Paper 2021*]

Ans. Dynamic resistance $= \dfrac{\Delta V}{\Delta I} = \dfrac{0.71 - 0.70}{10 \times 10^{-3}} = \dfrac{0.01}{10^{-2}} = 1\,\Omega$

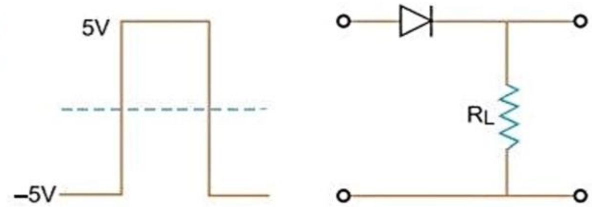
Q. 19. Why are elemental dopants for Silicon or Germanium usually chosen from group 13 or group 15? [*NCERT Exemplar*]

Ans. The size of dopant atoms should be such as not to distort the pure semiconductor lattice structure and yet easily contribute a charge carrier on forming covalent bonds with Si or Ge.

Q. 20. Sn, C, Si and Ge are all group 14 elements. Yet, Sn is a conductor, C is an insulator while Si and Ge are semiconductors. Why? [*NCERT Exemplar*]

Ans. If the valance and conduction bands overlap (no energy gap), the substance is referred as a conductor. For insulator the energy gap is large and for semiconductor the energy gap is moderate. The energy gap for Sn is 0 eV, for C is 5.4 eV, for Si is 1.1 eV and for Ge is 0.7 eV, related to their atomic size.

Q. 21. Draw the output signal in a *p-n* junction diode when a square input signal of 10 V as shown in the figure is applied across it.
[CBSE 2019 (55/5/1)]

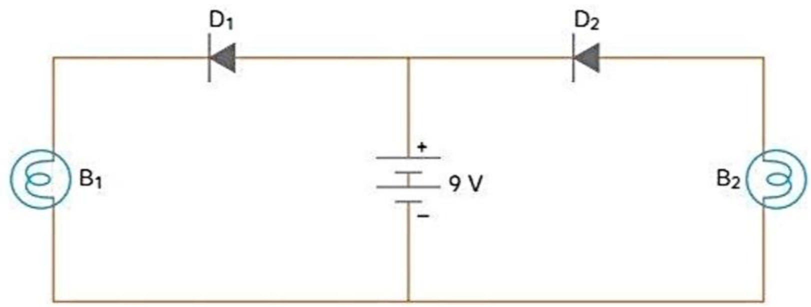


Ans.

Q. 22. How does one understand the temperature dependance of resistivity of a semiconductor?
[CBSE (F) 2010]

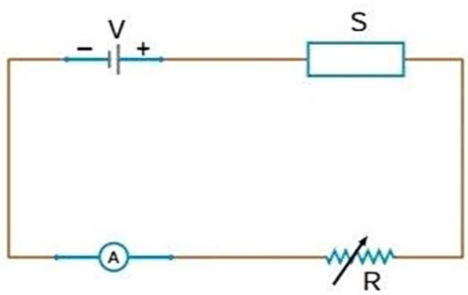
Ans. When temperature increases, covalent bonds of neighbouring atoms break and charge carrier become free to cause conduction, so resistivity of semi-conductor decreases with rise of temperature.

Q. 23. In the following diagram, which bulb out of B_1 and B_2 will glow and why? ***[CBSE (AI) 2017]***



Ans. Bulb B_1 will glow as diode D_1 is forward biased.

Q. 24. In the following diagram 'S' is a semiconductor. Would you increase or decrease the value of R to keep the reading of the ammeter A constant when S is heated? Give reason for your answer.
[CBSE (AI) 2017]



Ans.

When S is heated, the temperature increases. The resistivity decreases. The resistance of the circuit decreases so more current tend to flow. In order to keep the current value as constant the resistance R should be increased.
So R is increased to keep the ammeter reading as constant.

[Topper's Answer 2017]

Q. 25. What happens when a forward bias is applied to a *p-n* junction? ***[CBSE Panchkula 2015]***

Ans. The direction of the applied voltage (V) is opposite to the built-in potential V_0. As a result, depletion layer width decreases and the barrier height is reduced to $V_0 - V$.

Very Short Answer Questions

Each of the following questions are of 2 marks.

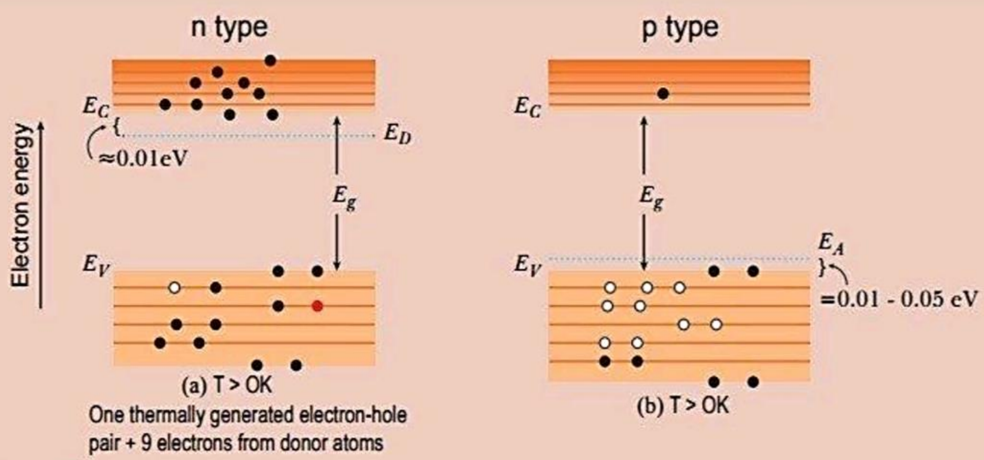
Q. 1. Distinguish between a metal and an insulator on the basis of energy band diagrams. *[CBSE (F) 2014]*

Ans.

	Metal	Insulators
(*i*)	Conduction band and valence band overlap each other.	There is large energy gap between conduction band and valence band.
(*ii*)	Conduction band is partially filled and valence band is partially empty.	Conduction band is empty. This is because no electrons can be excited to it from valence band.

Q. 2. Draw energy band diagrams of *n*-type and *p*-type semiconductors at temperature T > 0 K, depicting the donor and acceptor energy levels. Mention the significance of these levels. *[CBSE 2022 (55/1/1), Term-2, 2023 (55/2/1)]*

Ans.



1

Significance

n-type semiconductors – small energy gap between donor level and conduction band which can be easily covered by thermally excited electrons. 1

p- type semiconductors - small energy gap between acceptor level and valence band which can be easily covered by thermally excited electrons.

Alternatively

The conductivity of semiconductor is improved with the creation of donor and acceptor levels.

[CBSE Marking Scheme 2022 (55/1/1), Term-2]

Q. 3. Answer the following giving reasons:

(*a*) **A *p-n* junction diode is damaged by a strong current.**

(*b*) **Impurities are added in intrinsic semiconductors.** *[CBSE 2023 (55/2/1)]*

Ans. (*a*) When a strong current passes through the semiconductor it heats up the crystal and covalent bond are broken. Hence *p-n* junction diode is damaged.

(*b*) By the process of doping, impurities are added in intrinsic semiconductors to increase the conductivity.

Q. 4. How is forward biasing different from reverse biasing in a *p-n* junction diode?
[*CBSE Delhi 2011*]

Ans. **1. Forward Bias:**

(*i*) Within the junction diode the direction of applied voltage is opposite to that of built-in potential.

(*ii*) The current is due to diffusion of majority charge carriers through the junction and is of the order of milliamperes.

(*iii*) The diode offers very small resistance in the forward bias.

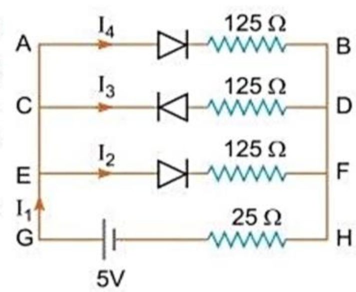
2. Reverse Bias:

(*i*) The direction of applied voltage and barrier potential is same.

(*ii*) The current is due to leakage of minority charge carriers through the junction and is very small of the order of μA

(*iii*) The diode offers very large resistance in reverse bias.

Q. 5. If each diode in figure has a forward bias resistance of 25 Ω and infinite resistance in reverse bias, what will be the values of current I_1, I_2, I_3 and I_4? **[*HOTS*] [*NCERT Exemplar*]**



Ans. I_3 is zero as the diode in that branch is reverse biased. Resistance in the branch *AB* and *EF* are each $(125 + 25)\ \Omega = 150\ \Omega$

As *AB* and *EF* are identical parallel branches, their effective resistance is $\frac{150}{2} = 75\ \Omega$

$\therefore$ Net resistance in the circuit $= (75 + 25)\ \Omega = 100\ \Omega$

$\therefore$ Current $I_1 = \frac{5}{100} = \mathbf{0.05\ A}$

As resistances of *AB* and *EF* are equal, and $I_1 = I_2 + I_3 + I_4$, $I_3 = 0$

$\therefore$ $I_2 = I_4 = \frac{0.05}{2} = \mathbf{0.025\ A}$

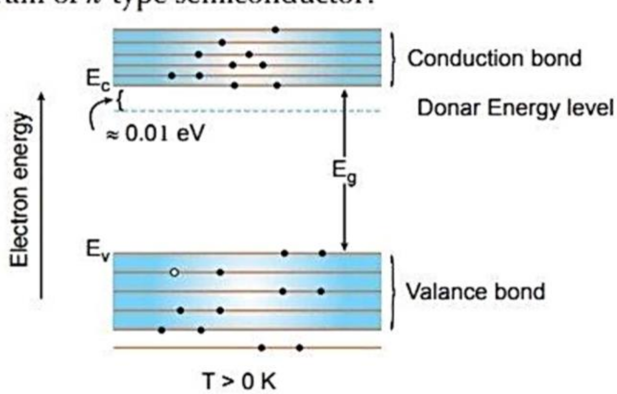
Q. 6. In a pure semiconductor crystal of Si, if antimony is added then what type of extrinsic semiconductor is obtained. Draw the energy band diagram of this extrinsic semiconductor so formed. **[*CBSE Sample Paper 2022, Term-2*]**

OR

A germanium crystal is doped with antimony. With the help of energy-band diagram, explain how the conductivity of the doped crystal is affected. **[*CBSE 2023 (55/4/1)*]**

Ans. As given in the statement antimony is added to pure Si/Ge crystal, then a *n*-type extrinsic semiconductor would be so obtained, Since antimony(Sb) is a pentavalent impurity. After doping with antimony, the number of conduction electrons can be made much larger than the number of holes. Due to this conductivity of the doped crystal increases.

Energy level diagram of *n*-type semiconductor:



Q. 7. A germanium *p-n* junction is connected to a battery with milliammeter in series. What should be the minimum voltage of battery so that current may flow in the circuit? **[*HOTS*]**

Ans. The internal potential barrier of germanium is 0.3 V, therefore to overcome this barrier the potential of battery should be equal to or more than 0.3 V.

Therefore, the minimum voltage of battery = **0.3 V.**

Q. 8. Briefly explain how the diffusion and drift currents contribute to formation of potential barrier in a *p-n* junction diode. **[*CBSE 2023 (55/1/1)*]**

OR

Explain briefly the two processes that occur in *p-n* junction region to create a potential barrier. **[*CBSE 2020 (55/3/1)*]**

Ans. **Diffusion:** During the formation of *p-n* junction, due to the concentration gradient across the *p* and *n* sides, the motion of majority charge carriers give rise to diffusion current. **1**

Drift: Due to the electric field developed at the junction, the motion of the minority charge carriers due to electric field is called drift. **1**

With the passage of time, diffusion current decreases whereas drift current increases and balance each other. This, creates a potential barrier. **[*CBSE Marking Scheme 2020 (55/3/1)*]**

Q. 9. Explain the property of a *p-n* junction which makes it suitable for rectifying alternating voltages. Differentiate between a half-wave and a full-wave rectifier. **[*CBSE 2023 (55/3/1)*]**

Ans. Rectification means conversion of *ac* into *dc*. A *p-n* diode acts as a rectifier because an *ac* changes polarity periodically and a *p-n* diode allows the current to pass only when it is forward biased. This characteristics property makes the diode suitable for rectification.

Difference between Half wave and Full wave rectifier

	Half wave rectifier	Full wave rectifier
(*i*)	It converting the one-half cycles of *AC* input to *DC* output.	It converting both the half cycles or complete full cycle of *AC* input in to *DC* output.
(*ii*)	Ripple factor of a half-wave rectifier is more.	Ripple factor of a full wave rectifier is less.
(*iii*)	Single *p–n* junction diode is used for rectification.	At least two or four diode may used for rectification depending on the type of circuit.

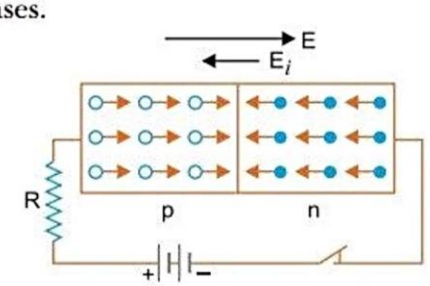
Q. 10. What is meant by doping of an intrinsic semiconductor? Name the two types of atoms used for doping of Ge/Si. **[*CBSE 2022 (55/3/1), Term-2*]**

Ans. **Doping:** The deliberate addition of a desirable impurity in pure Si/Ge semiconductor to enhance conductivity is called doping.

Types of atoms: (*i*) Pentavalent – Arsenic (As) (*ii*) Trivalent – Boron (B).

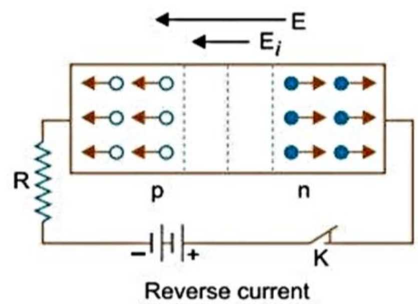
Q. 11. What will the effect of (*i*) forward biasing, and (*ii*) reverse biasing be on the width of depletion layer in *p-n* junction diode? **[*CBSE 2023 (55/4/1)*]**

Ans. (*i*) Under forward biasing the applied potential difference causes a field which acts opposite to the potential barrier. This results in reducing the potential barrier, and hence the width of depletion layer decreases.



Forward current

(*ii*) Under reverse biasing the applied potential difference causes a field which is in the same direction as the field due to internal potential barrier. This results in an increase in barrier voltage and hence the width of depletion layer increases.



Short Answer Questions

Each of the following questions are of 3 marks.

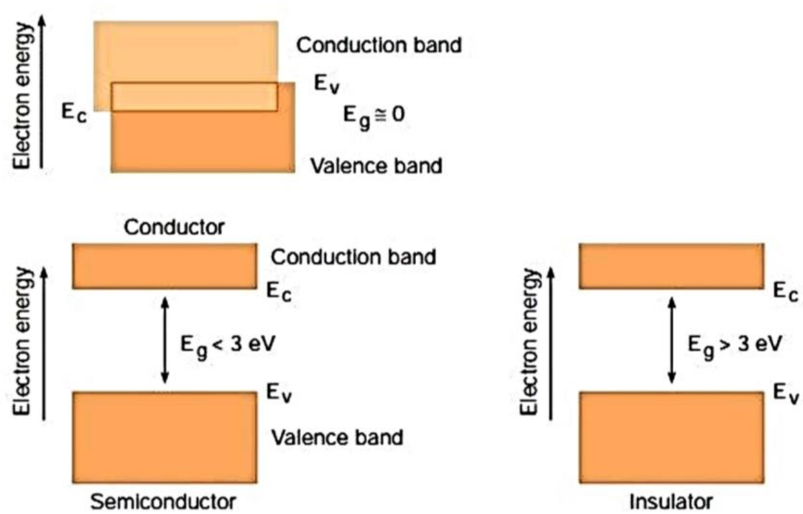
Q. 1. What are energy bands? Write any two distinguishing features between conductors, semiconductors and insulators on the basis of energy band diagrams.

[*CBSE (AI) 2014, North 2016*]

OR

Draw the necessary energy band diagrams to distinguish between conductors, semiconductors and insulators. How does the change in temperature affect the behaviour of these materials? Explain briefly. **[*CBSE Patna 2015, 2020 (55/4/1)*]**

Ans. **Energy Bands:** In a solid, the energy of electrons lie within certain range. The energy levels of allowed energy are in the form of bands, these bands are separated by regions of forbidden energy called band gaps.



Distinguishing features:

(*a*) In conductors: Valence band and conduction band overlap each other.

In semiconductors: Valence band and conduction band are separated by a small energy gap.

In insulators: They are separated by a large energy gap.

(*b*) In conductors: Large number of free electrons are available in conduction band.

In semiconductors: A very small number of electrons are available for electrical conduction.

In insulators: Conduction band is almost empty *i.e.*, no electron is available for conduction.

Effect of Temperature:

(*i*) **In conductors:** At high temperature, the collision of electrons become more frequent with the atoms/molecules at lattice site in the metals as a result the conductivity decreases (or resistivity increases).

(*ii*) **In semiconductors:** As the temperature of the semiconducting material increases, more electron hole pairs becomes available in the conduction band and valance band, and hence the conductivity increases or the resistivity decreases.

(*iii*) **In insulators:** The energy band between conduction band and valance band is very large, so it is unsurpassable for small temperature rise. So, there is no change in their behaviour.

Q. 2. Distinguish between 'intrinsic' and 'extrinsic' semiconductors.

[*CBSE Delhi 2015, (F) 2017, 2023 (55/1/1)*]

Ans.

	Intrinsic semiconductor	Extrinsic semiconductor
(*i*)	It is a semiconductor in pure form.	It is a semiconductor doped with trivalent or pentavalent impurity atoms.
(*ii*)	Intrinsic charge carriers are electrons and holes with equal concentration.	The two concentrations are unequal in it. There is excess of electrons in *n*-type and excess of holes in *p*-type semiconductors.
(*iii*)	Current due to charge carriers is feeble (of the order of μA).	Current due to charge carriers is significant (of the order of mA).

Q. 3. Name the important process that occurs during the formation of a *p-n* junction. Explain briefly, with the help of a suitable diagram, how a *p-n* junction is formed. Define the term 'barrier potential'. [*CBSE (F) 2011, Central 2016*]

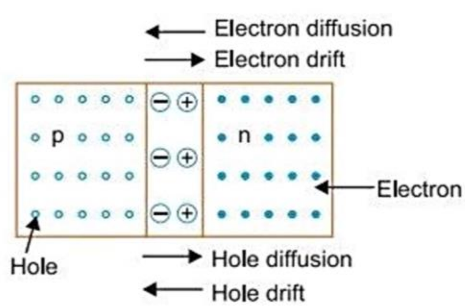
OR

Describe briefly, with the help of a diagram, the role of the two important processes involved in the formation of a *p-n* junction.

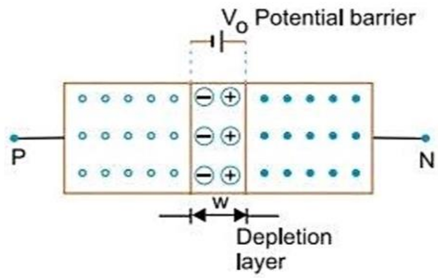
[*CBSE (AI) 2012, Bhubaneshwar 2015, 2020 (55/4/1), 2023 (55/3/1), (55/4/1)*]

Ans. Two important processes occurring during the formation of a *p-n* junction are (*i*) diffusion and (*ii*) drift.

(*i*) **Diffusion:** In *n*-type semiconductor, the concentration of electrons is much greater as compared to concentration of holes; while in *p*-type semiconductor, the concentration of holes is much greater than the concentration of electrons. When a *p-n* junction is formed, then due to concentration gradient, the holes diffuse from *p*-side to *n*-side ($p \rightarrow n$) and electrons diffuse from *n*-side to *p*-side ($n \rightarrow p$). This motion of charge carriers gives rise to diffusion current across the junction.



(*ii*) **Drift:** The drift of charge carriers occurs due to electric field. Due to built in potential barrier, an electric field directed from *n*-region to *p*-region is developed across the junction. This field causes motion of electrons on *p*-side of the junction to *n*-side and motion of holes on *n*-side of junction to *p*-side. Thus a drift current starts. This current is opposite to the direction of **diffusion current.**



Potential barrier: During the formation of a *p-n* junction the electrons diffuse from *n*-region to *p*-region and holes diffuse from *p*-region to *n*-region. This forms recombination of charge carriers. In this process immobile positive ions are collected at a junction toward *n*-region and negative ions at a junction toward *p*-region. This causes a potential difference across the unbiased junction. This is called potential barrier.

Q. 4. Draw $V - I$ characteristics of a p–n junction diode. Answer the following questions, giving reasons:

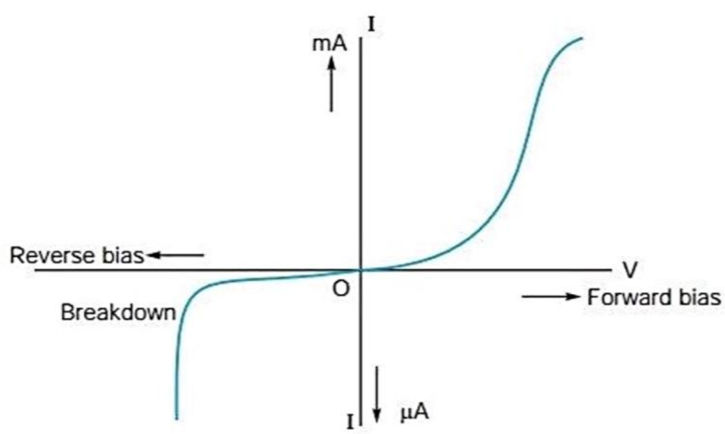
(*i*) Why is the current under reverse bias almost independent of the applied potential upto a critical voltage?

(*ii*) Why does the reverse current show a sudden increase at the critical voltage?

[*CBSE (AI) 2013, CBSE 2019*]

Ans. (*i*) In the reverse biasing, the current of order of μA is due to movement/drifting of minority charge carriers from one region to another through the junction.

A small applied voltage is sufficient to sweep the minority charge carriers through the junction. So, reverse current is almost independent of critical voltage.



(*ii*) At critical voltage (or breakdown voltage), a large number of covalent bonds break, resulting in the increase of large number of charge carriers. Hence, current increases at critical voltage.

Q. 5. The current in the forward bias is known to be more (~mA) than the current in the reverse bias (~μA). What is the reason, then, to operate the photodiode in reverse bias?

[*HOTS*][*CBSE Delhi 2012*]

Ans. Consider the case of *n*-type semiconductor. The majority carrier (electron) density is larger than the minority hole density, *i.e.*, $n >> p$.

On illumination, the no. of both types of carriers would equally increase in number as

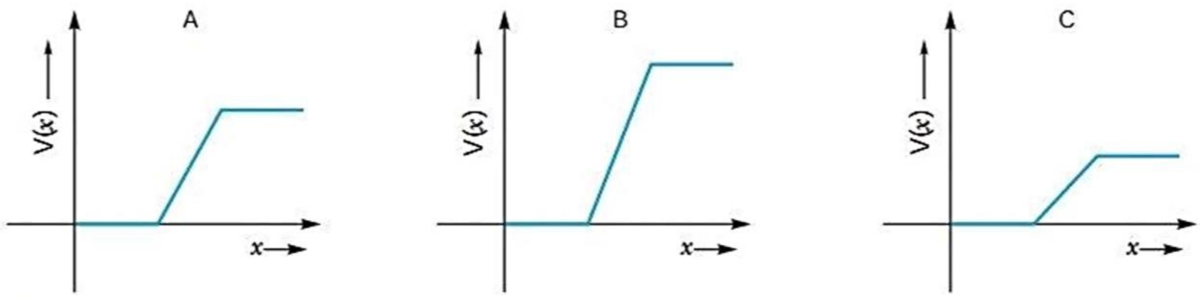
$n' = n + \Delta n, p' = p + \Delta p$

But $\Delta n = \Delta p$ and $n >> p$

Hence, the fractional change in majority carrier, *i.e*, $\frac{\Delta n}{n} << \frac{\Delta p}{p}$ (fractional change in minority carrier)

Fractional change due to photo-effects on minority carrier dominated reverse bias current is more easily measurable than the fractional change in majority carrier dominated forward bias current. Hence photodiodes are used in reverse bias condition for measuring light intensity.

Q. 6. The graph of potential barrier versus width of depletion region for an unbiased diode is shown in *A*. In comparison to *A*, graphs *B* and *C* are obtained after biasing the diode in different ways. Identify the type of biasing in *B* and *C* and justify your answer. [*CBSE Sample Paper 2016, 2023*]



Ans. B : Reverse biased

Justification: When an external voltage V is applied across the semiconductor diode such that n-side is positive and p-side is negative, the direction of applied voltage is same as the direction of barrier potential. As a result, the barrier height increases and the depletion region widens due to the change in the electric field. The effective barrier height under reverse bias is (V_0+V).

C : Forward biased

Justification: When an external voltage V is applied across a diode such that p-side is positive and n-side is negative, the direction of applied voltage (V) is opposite to the barrier potential (V_0). As a result, the depletion layer width decreases and the barrier height is reduced. The effective barrier height under forward bias is $(V_0 - V)$.

Q. 7. A semiconductor has equal electron and hole concentration of 2×10^8 / m^3. On doping with a certain impurity, the hole concentration increases to 4×10^{10} / m^3.

(*i*) What type of semiconductor is obtained on doping?

(*ii*) Calculate the new electron and hole concentration of the semiconductor.

(*iii*) How does the energy gap vary with doping?

Ans. Given $n_e = 2 \times 10^8$ / m^3, $n_h = 4 \times 10^{10}$ / m^3

(*i*) The majority charge carriers in doped semiconductor are holes, so semiconductor obtained is p-type semiconductor.

(*ii*) $n_e n_h = n_i^2 \Rightarrow n_e = \frac{n_i^2}{n_h} = \frac{(2\times10^8)^2}{4\times10^{10}} = \mathbf{10^6/m^3}$

New electron concentration = 10^6 / m^3

hole concentration = 4×10^{10} / m^3

(*iii*) Energy gap decreases on doping.

Long Answer Questions

Each of the following questions are of 5 marks.

Q. 1. (*a*) **State briefly the processes involved in the formation of *p-n* junction explaining clearly how the depletion region is formed.**

(*b*) **Using the necessary circuit diagrams, show how the V–I characteristics of a *p-n* junction are obtained in (*i*) Forward biasing (*ii*) Reverse biasing**

How are these characteristics made use of in rectification? **[*CBSE Delhi 2014*]**

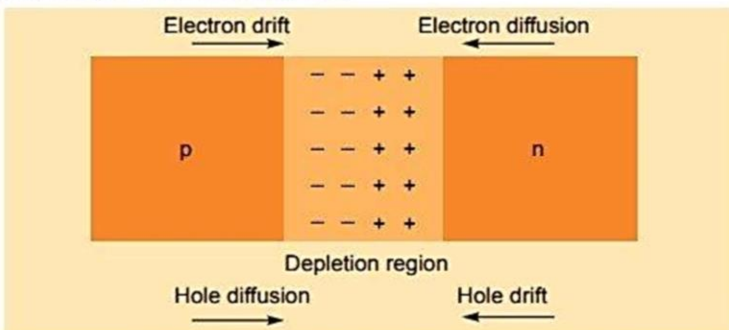
OR

Draw the circuit arrangement for studying the *V–I* characteristics of a *p-n* junction diode (*i*) in forward bias and (*ii*) in reverse bias. Draw the typical *V–I* characteristics of a silicon diode. Describe briefly the following terms: **[*CBSE 2023 (55/1/1)*]**

(*i*) **"minority carrier injection" in forward bias**

(*ii*) **"breakdown voltage" in reverse bias.** **[*CBSE Chennai 2015*]**

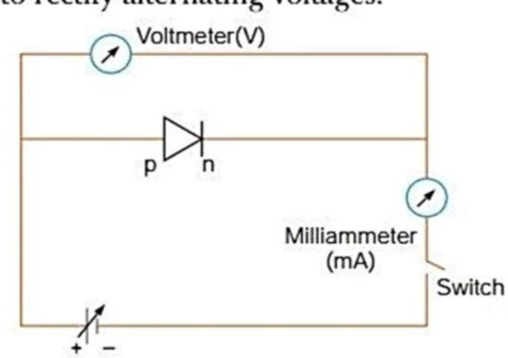
Ans. (*a*)



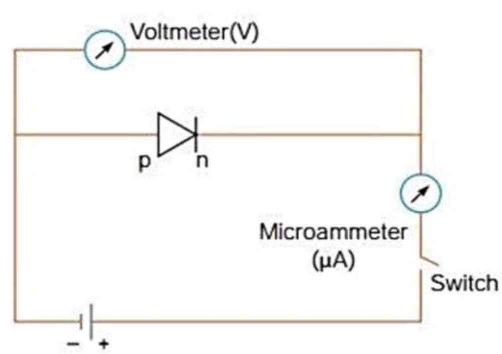
Two processes occur during the formation of a *p-n* junction are diffusion and drift. Due to the concentration gradient across *p* and *n*-sides of the junction, holes diffuse from *p*-side to *n*-side ($p \rightarrow n$) and electrons diffuse from *n*-side to *p*-side ($n \rightarrow p$). This movement of charge carriers leaves behind ionised acceptors (negative charge immobile) on the *p*-side and donors (positive charge immobile) on the *n*-side of the junction. This space charge region on either side of the junction together is known as depletion region.

(*b*) The circuit arrangement for studying the *V–I* characteristics of a diode are shown in Fig. (*a*) and (*b*). For different values of voltages the value of current is noted. *A* graph between *V* and *I* is obtained as in Figure (*c*).

From the *V–I* characteristic of a junction diode it is clear that it allows current to pass only when it is forward biased. So if an alternating voltage is applied across a diode the current flows only in that part of the cycle when the diode is forward biased. This property is used to rectify alternating voltages.



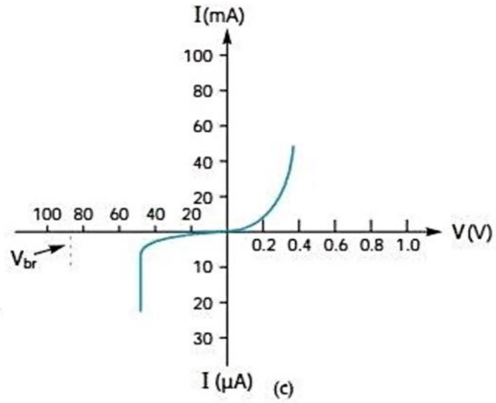
(a)



(b)

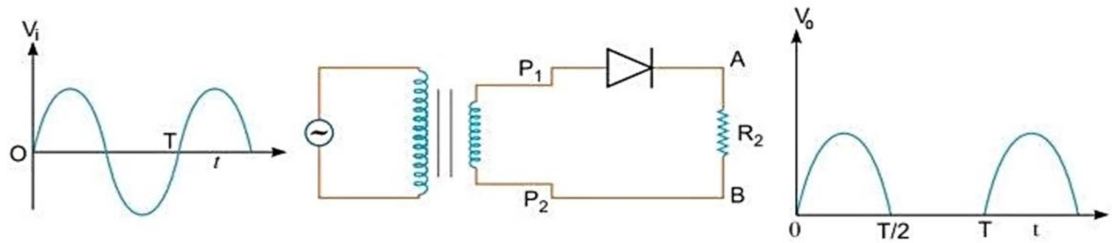
(*i*) **Minority Carrier Injection:** Due to the applied voltage, electrons from *n*-side cross the depletion region and reach *p*-side (where they are minority carriers). Similarly, holes from *p*-side cross this junction and reach the *n*-side (where they are minority carriers). This process under forward bias is known as minority carrier injection.

(*ii*) **Breakdown Voltage:** It is a critical reverse bias voltage at which current is independent of applied voltage.



Q. 2. Explain, with the help of a circuit diagram, the working of a *p-n* junction diode as a half-wave rectifier. [*CBSE (AI) 2014*]

Ans.



Working

(*i*) During positive half cycle of input alternating voltage, the diode is forward biased and a current flows through the load resistor R_L and we get an output voltage.

(*ii*) During other negative half cycle of the input alternating voltage, the diode is reverse biased and it does not conduct (under break down region).

Hence, *ac* voltage can be rectified in the pulsating and unidirectional voltage.

Q. 3. State the principle of working of *p-n* diode as a rectifier. Explain with the help of a circuit diagram, the use of *p-n* diode as a full wave rectifier. Draw a sketch of the input and output waveforms. [*CBSE Delhi 2012, 2020 (55/3/2)*]

OR

Draw a circuit diagram of a full wave rectifier. Explain the working principle. Draw the input/output waveforms indicating clearly the functions of the two diodes used.

[*CBSE (AI) 2011, 2020 (55/1/3)*]

OR

With the help of a circuit diagram, explain the working of a junction diode as a full wave rectifier. Draw its input and output waveforms. Which characteristic property makes the junction diode suitable for rectification? [*CBSE Ajmer 2015, North 2016, 2023 (55/4/1)*]

OR

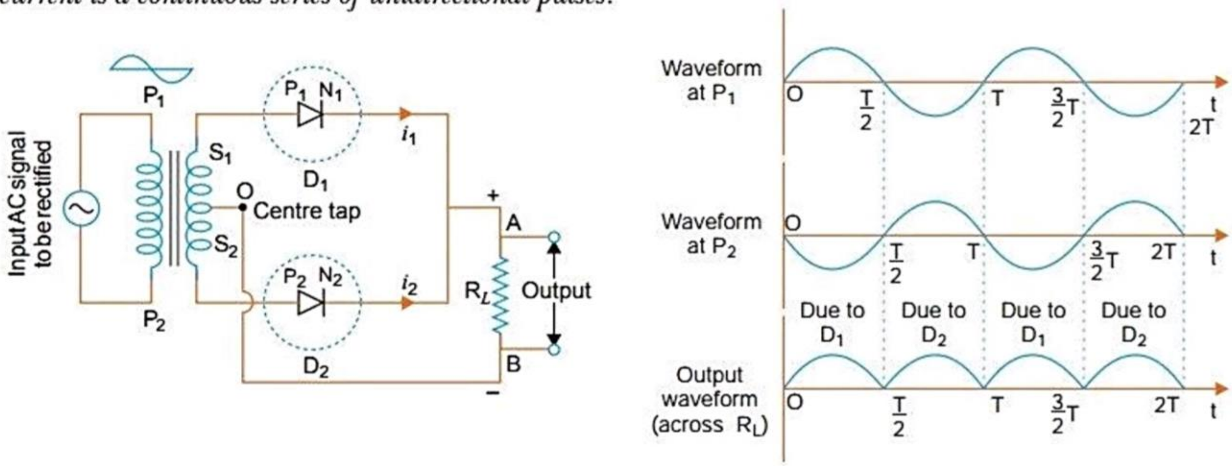
Draw the circuit diagram of a full wave rectifier and explain its working. Also give the input and output waveforms. [*CBSE Delhi 2019, 2020, (55/1/3), 2022 (55/2/1), Term-2*]

OR

Explain with a proper diagram how an ac signal can be converted into *dc* (pulsating) signal with output frequency as double than the input frequency using *p–n* junction diode. Give its input and output waveforms. [*CBSE Sample Paper 2022, Term-2*]

Ans. **Rectification:** Rectification means conversion of *ac* into *dc*. A *p-n* diode acts as a rectifier because an *ac* changes polarity periodically and a *p-n* diode allows the current to pass only when it is forward biased. This makes the diode suitable for rectification.

Working: The ac input voltage across secondary S_1 and S_2 changes polarity after each half cycle. Suppose during the first half cycle of input ac signal, the terminal S_1 is positive relative to centre tap O and S_2 is negative relative to O. Then diode D_1 is forward biased and diode D_2 is reverse biased. Therefore, diode D_1 conducts while diode D_2 does not. The direction of current (i_1) due to diode D_1 in load resistance R_L is directed from A to B In next half cycle, the terminal S_1 is negative and S_2 is positive relative to centre tap O. The diode D_1 is reverse biased and diode D_2 is forward biased. Therefore, diode D_2 conducts while D_1 does not. The direction of current (i_2) due to diode D_2 in load resistance R_L is still from A to B. Thus, the current in load resistance R_L is in the same direction for both half cycles of input ac voltage. Thus *for input ac signal the output current is a continuous series of unidirectional pulses.*



In a full wave rectifier, if input frequency is f hertz, then output frequency will be $2f$ hertz because for each cycle of input, two positive half cycles of output are obtained.

Q. 4. (*a*) **Distinguish between an intrinsic semiconductor and a *p*-type semiconductor. Give reason why a *p*-type semiconductor is electrically neutral, although $n_h >> n_e$.**

(*b*) **Explain, how the heavy doping of both *p*-and *n*-sides of a *p*-*n* junction diode results in the electric field of the junction being extremely high even with a reverse bias voltage of a few volts.** **[*CBSE (F) 2013*]**

Ans. (*a*)

	Intrinsic semiconductor	***p*-type semiconductor**
(*i*)	It is a semiconductor in pure form.	It is a semiconductor doped with trivalent impurity atoms (Like Al, Ga, *etc*.).
(*ii*)	Intrinsic charge carriers are electrons and holes with equal concentration.	There is excess of holes in *p*-type semiconductors as majority charge carrier.
(*iii*)	Current due to charge carriers is feeble (of the order of μA).	Current due to charge carriers is significant (of the order of mA).

When the trivalent imurities are doped in to the tetravalent pure semiconductor like Si or Ge then the fourth electron of the Si or Ge needs to be bounded then the electron in the outermost shell of the Si or Ge can jump in to the vacancy and create hole on its own atom. But the number of the electrons and holes are same in magnitude and apposite in sign. Hence a *p*-type semiconductor is electrically neutral.

(*b*) If *p*-type and *n*-type semiconductor are heavily doped. Then due to diffusion of electrons from *n*-region to *p*-region, and of holes from *p*-region to *n*-region, a depletion region formed of size of order less than 1 μm. The electric field directing from *n*-region to *p*-region produces a reverse bias voltage of about 5 V and electric field becomes very large.

$$E = \frac{\Delta V}{\Delta x} = \frac{5\text{V}}{1\mu\text{m}} \approx 5 \times 10^6 \text{ V/m}$$

Questions for Practice

1. **Choose and write the correct option in the following questions.**

(*i*) Carbon, silicon and germanium have four valence electrons each. These are characterised by valence and conduction bands, separated by energy band gap respectively equal to $(E_g)_C$, $(E_g)_{Si}$ and $(E_g)_{Ge}$. Which of the following statement is true?

(*a*) $(E_g)_{Si} < (E_g)_{Ge} < (E_g)_C$ (*b*) $(E_g)_C < (E_g)_{Ge} > (E_g)_{Si}$
(*c*) $(E_g)_C > (E_g)_{Si} > (E_g)_{Ge}$ (*d*) $(E_g)_C = (E_g)_{Si} = (E_g)_{Ge}$

(*ii*) If a *p-n* junction diode is reverse biased, *[CBSE 2023 (55/3/1)]*

(*a*) the potential barrier is lowered. (*b*) the potential barrier remains unaffected.
(*c*) the potential barrier is raised. (*d*) the current is mainly due to majority carriers.

(*iii*) When a forward bias is applied to a *p-n* junction, it

(*a*) raises the potential barrier (*b*) reduces the majority carrier current to zero
(*c*) lowers the potential barrier (*d*) none of the above

(*iv*) Pieces of copper and of silicon are initially at room temperature. Both are heated to temperature *T*. The conductivity of *[CBSE 2023 (55/2/1)]*

(*a*) both increases (*b*) both decreases
(*c*) copper increases and silicon decreases (*d*) copper decreases and silicon increases

(*v*) The formation of depletion region in a *p-n* junction diode is due to *[CBSE 2023 (55/2/1)]*

(*a*) movement of dopant atoms (*b*) diffusion of both electrons and holes
(*c*) drift of electrons only (*d*) drift of holes only

2. ***In the following questions, a statement of Assertion (A) is followed by a statement of Reason (R). Choose the correct answer out of the following choices.***

(a) ***Both A and R are true and R is the correct explanation of A.***
(b) ***Both A and R are true but R is not the correct explanation of A.***
(c) ***A is true but R is false.***
(d) ***A is false and R is also false.***

Assertion (*A*) : A *p-n* junction diode can be used even at ultra high frequencies.
Reason (*R*) : Capacitive reactance of *p-n* junction diode increases as frequency increases.

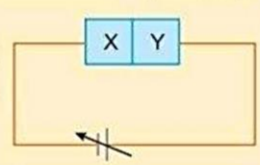
3. Explain the formation of depletion region in a *p-n* junction. *[CBSE Sample Paper 2022 (55/2/1)]*

4. Why is an intrinsic semiconductor deliberately conversed into an extrinsic semiconductor by adding impurity atoms? *[CBSE 2020 (55/3/1)]*

5. Draw the circuit arrangement for studying the *V-I* characteristics of a *p-n* junction diode in forward bias and reverse bias. Show the plot of *V-I* characteristic of a silicon diode. *[CBSE 2023 (55/1/1)]*

6. What happens when a forward bias is applied to a *p-n* junction?

7. Two semiconductor materials *X* and *Y* shown in the alongside figure, are made by doping a germanium crystal with indium and arsenic respectively. The two are joined end to end and connected to a battery as shown.

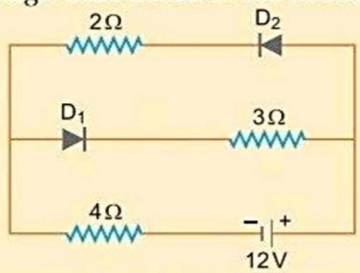


(*i*) Will the junction be forward biased or reverse biased?
(*ii*) Sketch a *V-I* graph for this arrangement.

8. Draw the energy band diagram when intrinsic semiconductor (Ge) is doped with impurity atoms of Antimony (Sb). Name the extrinsic semiconductor so obtained and majority charge carriers in it. *[CBSE Sample Paper 2021, 2022, Term-2]*

9. Explain the terms 'depletion layer' and 'potential barrier' in a *p-n* junction diode. How are the (*a*) width of depletion layer, and (*b*) value of potential barrier affected when the *p-n* junction is forward biased? **[*CBSE 2020 (55/1/1)*]**

10. The circuit shown in the figure has two oppositely connected ideal diodes connected in parallel. Find the current flowing through each diode in the circuit.



11. Write two characteristic features to distinguish between *n*-type and *p*-type semiconductors. **[*CBSE (F) 2012*]**

12. Draw energy band diagrams of an *n*-type and *p*-type semiconductor at temperature $T > 0$ K. Mark the donor and acceptor energy levels with their energies. **[*CBSE (F) 2014, 2020 (55/3/3)*]**

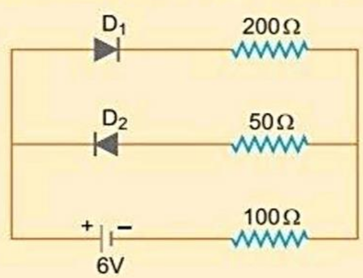
13. Three photo diodes D_1, D_2 and D_3 are made of semiconductors having band gaps of 2.5 eV, 2 eV and 3 eV, respectively. Which ones will be able to detect light of wavelength 6000 Å? **[*HOTS*] [*NCERT Exemplar*]**

14. Draw $V - I$ characteristics of *p-n* junction diode. Explain how these characteristics make a diode suitable for rectification. **[*CBSE 2023 (55/4/1)*]**

15. Write the two processes that take place in the formation of *p-n* junction. Explain with the help of a diagram, the formation of depletion region and barrier potential in a *p-n* junction. **[*CBSE Delhi 2017*]**

16. (*a*) Draw *V-I* characteristics of a *p-n* junction diode. Explain, why the current under reverse bias is almost independent of the applied voltage up to the critical voltage. **[*CBSE 2020 (55/2/1)*]**

(*b*) The circuit shown in the figure contains two diodes each with a forward resistance of 50 Ω and infinite backward resistance. Calculate the current in the 100 Ω resistance.



Answers

1. (*i*) (*c*) (*ii*) (*c*) (*iii*) (*c*) (*iv*) (*d*) (*v*) (*b*)
2. (*c*)

10. 2 A 16. (*b*) 0.0171 A